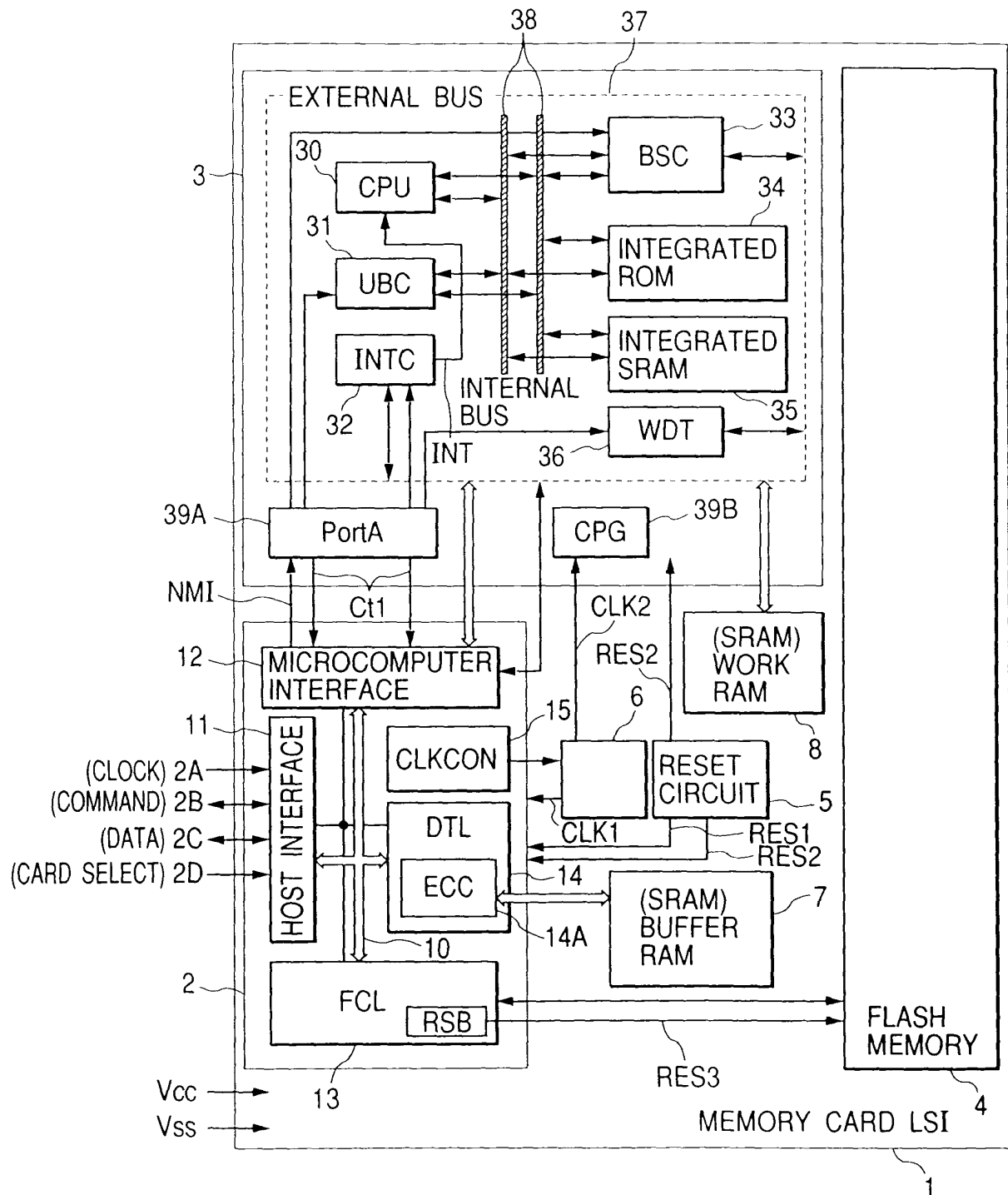
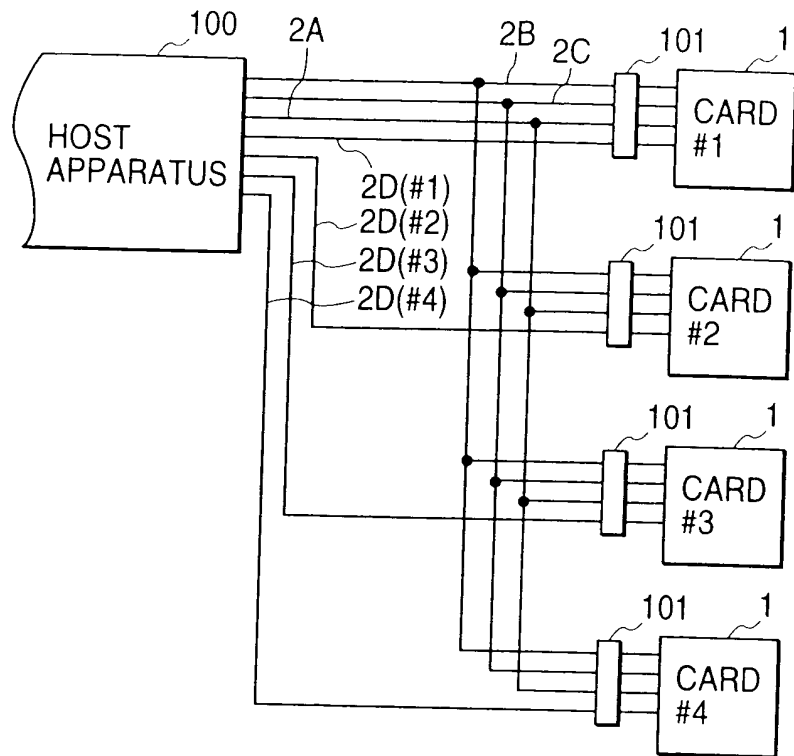
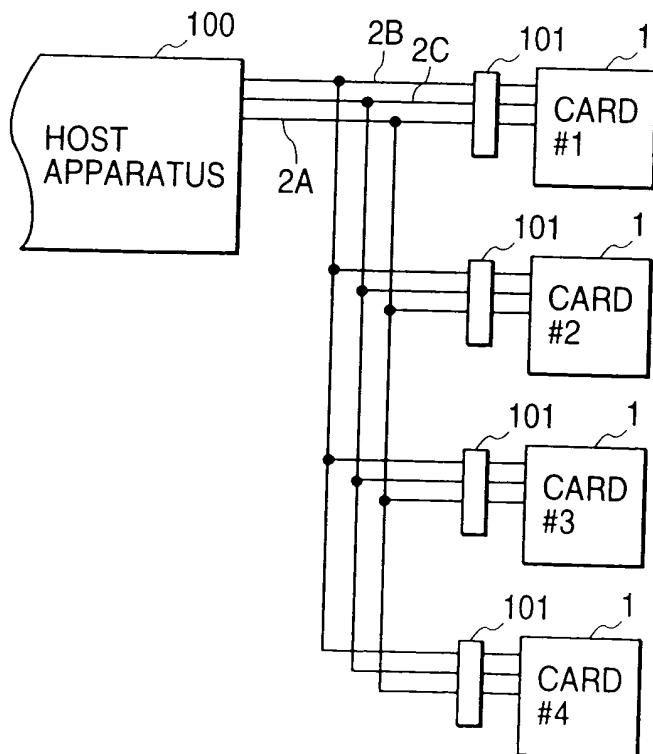


FIG. 1



**FIG. 2****FIG. 3**

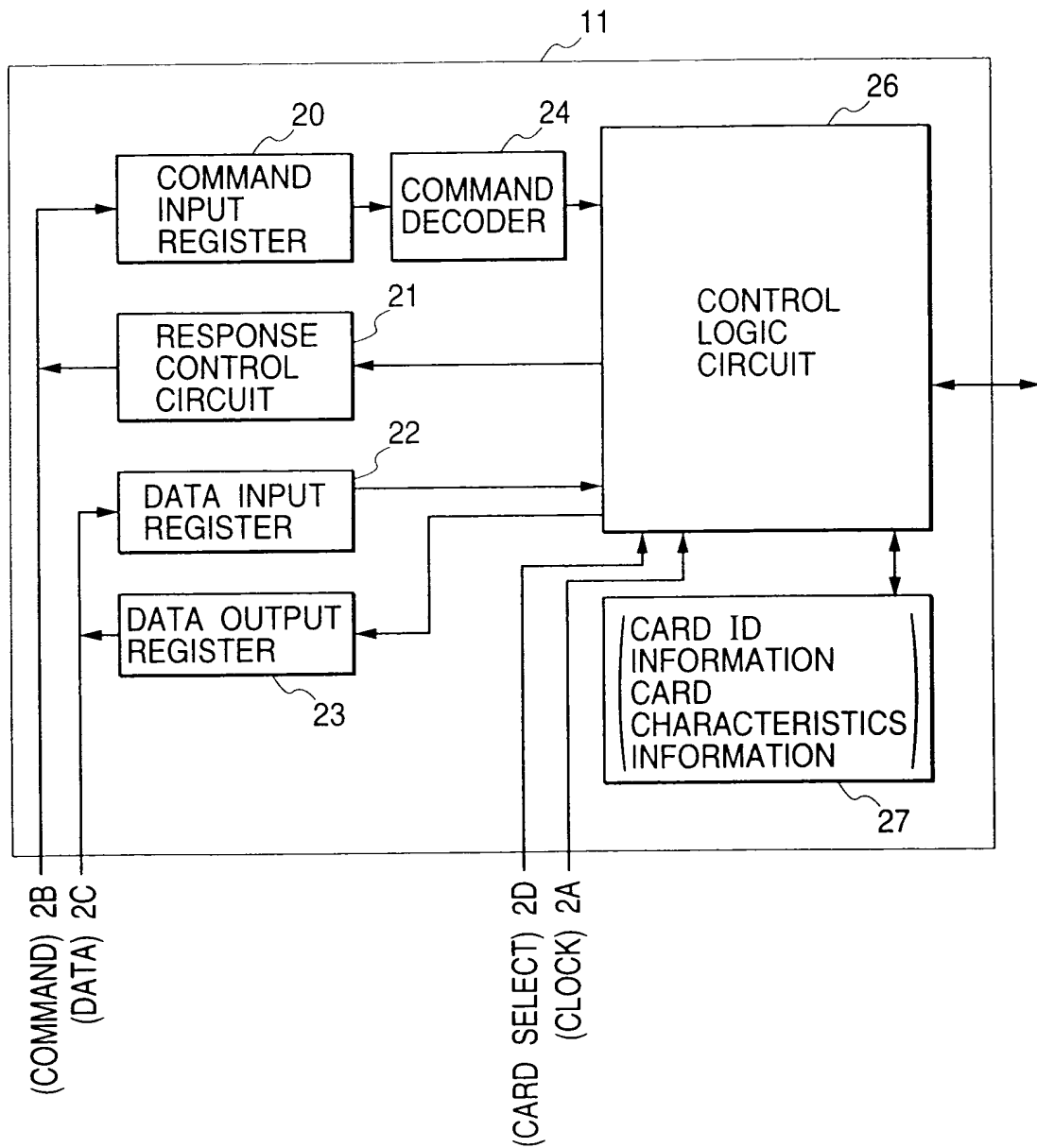
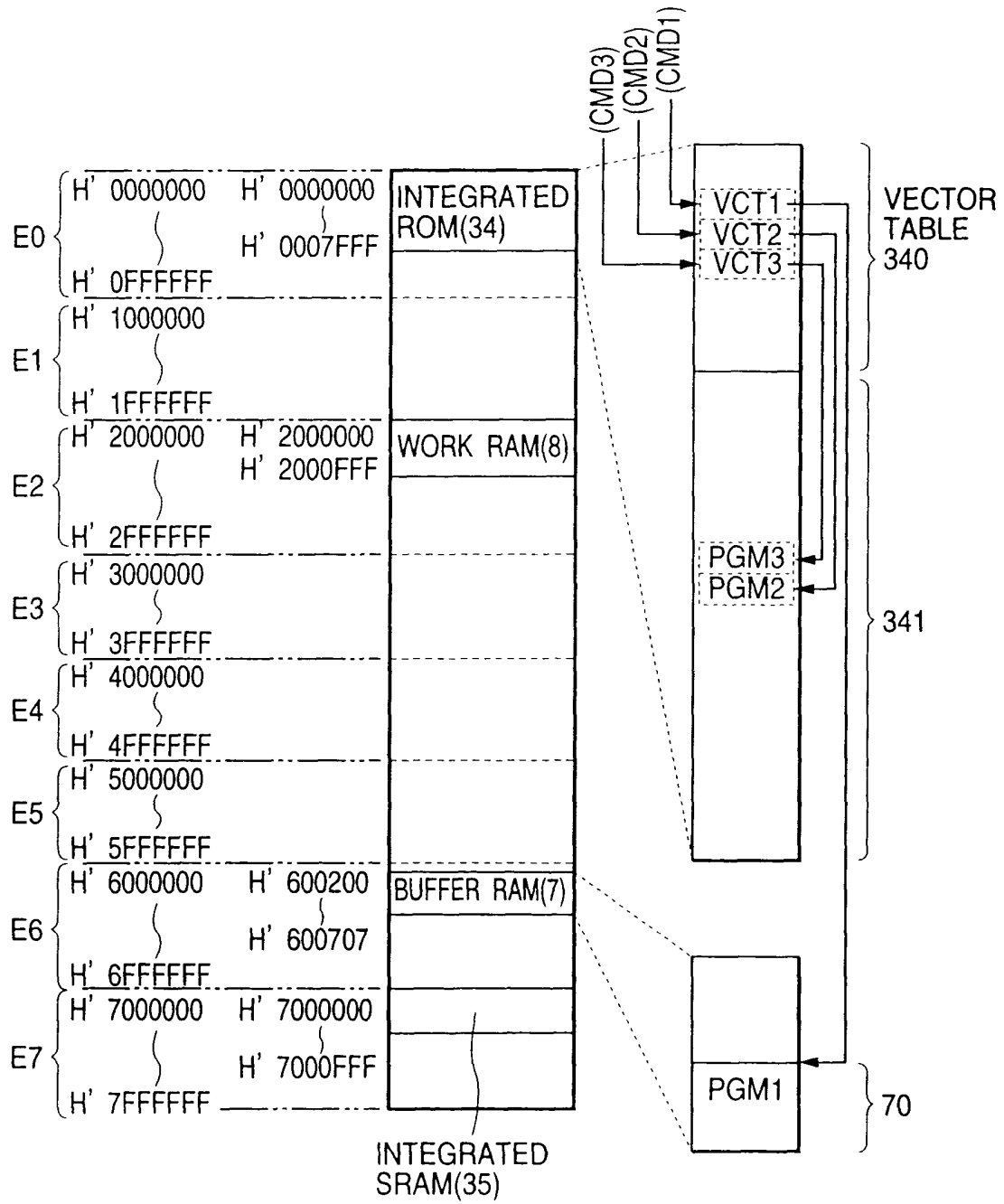
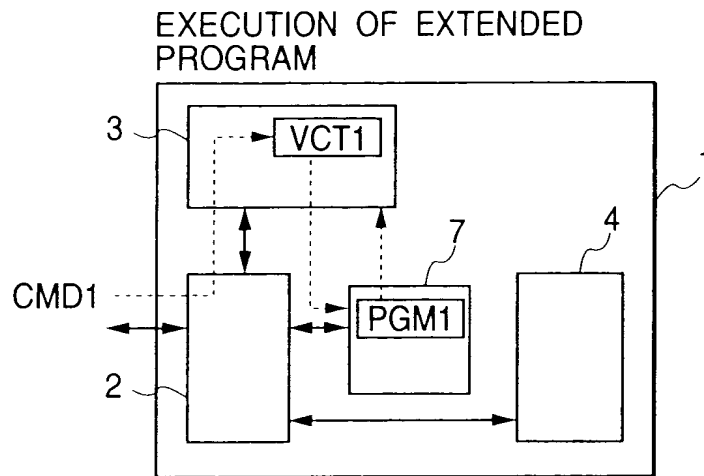
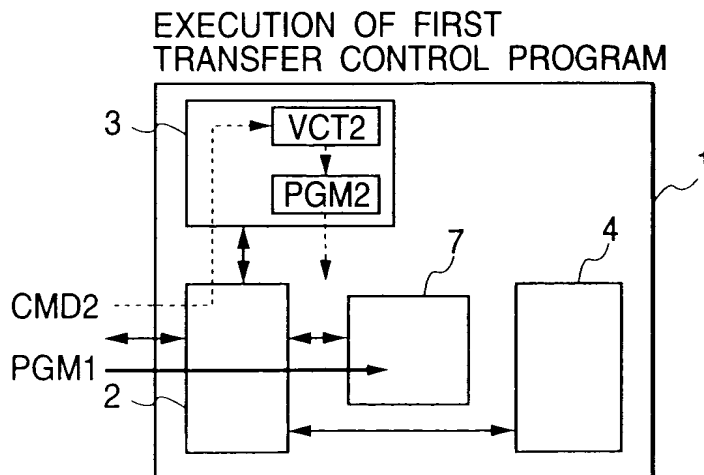
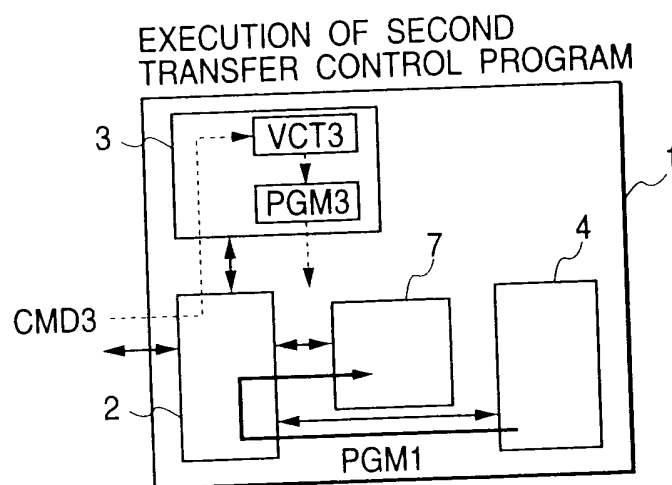
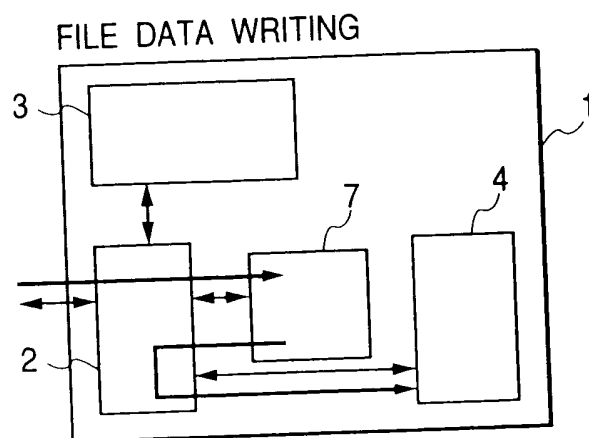
*FIG. 4*

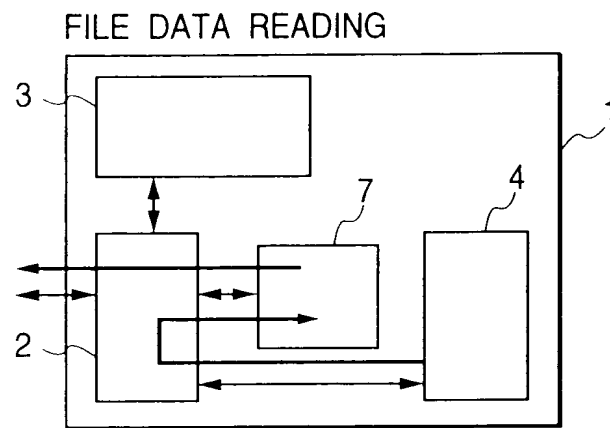
FIG. 5



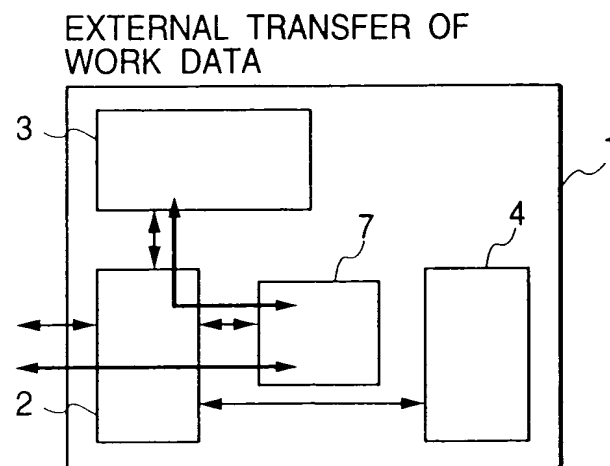
*FIG. 6**FIG. 7*

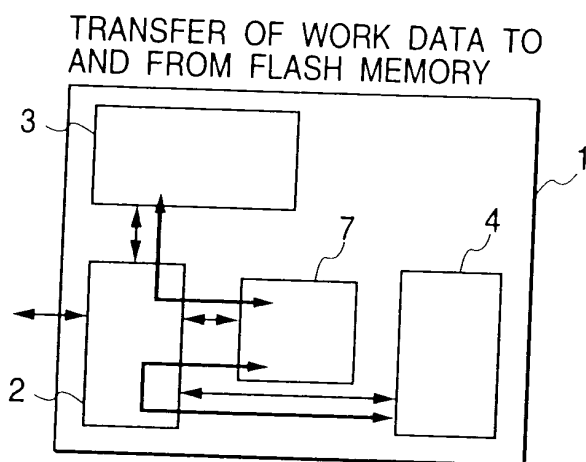
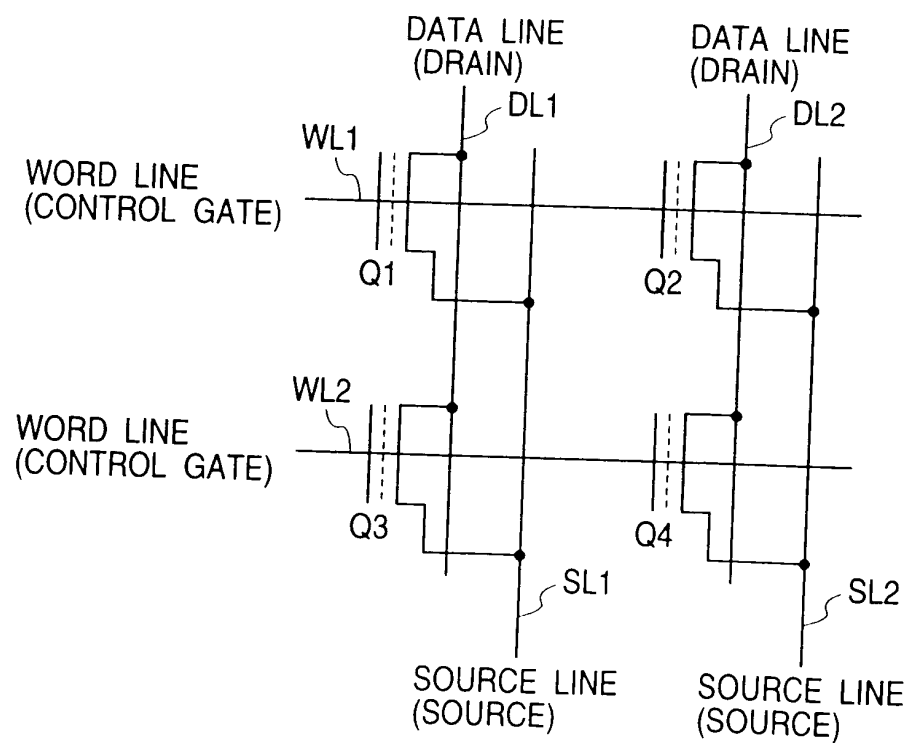
**FIG. 8****FIG. 9**

*FIG. 10*

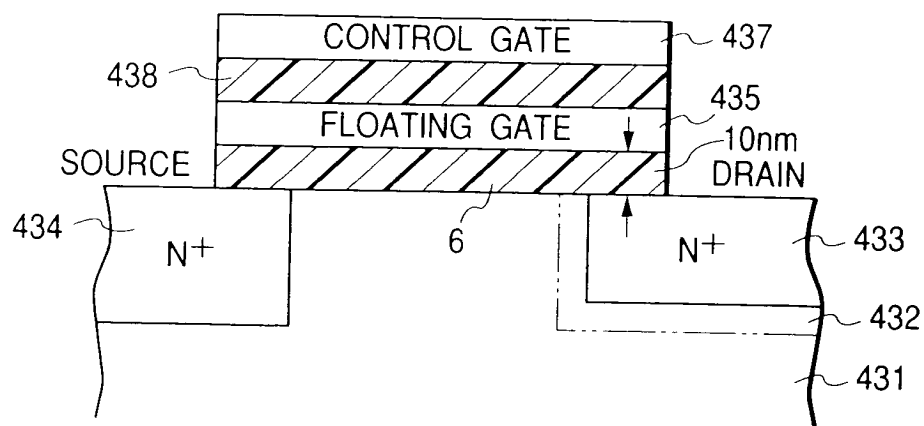
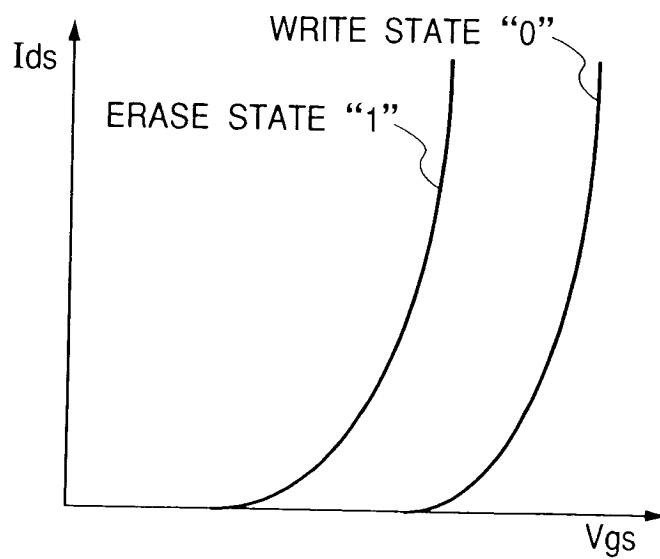


*FIG. 11*



*FIG. 12**FIG. 14*



*FIG. 13(A)**FIG. 13(B)*

*FIG. 15(A)*

PROGRAM

MEMORY CELL	SELECTED/ UNSELECTED	SOURCE	DRAIN	CONTROL GATE
Q1	SELECTED	0V	6V	12V
Q2	UNSELECTED	0V	0V	12V
Q3	UNSELECTED	0V	6V	0V
Q4	UNSELECTED	0V	0V	0V

*FIG. 15(B)*

ERASE (POSITIVE VOLTAGE TYPE)

MEMORY CELL	SELECTED/ UNSELECTED	SOURCE	DRAIN	CONTROL GATE
Q1,Q3	SELECTED	12V	0V	0V
Q2,Q4	UNSELECTED	0V	0V	0V

*FIG. 15(C)*

ERASE (NEGATIVE VOLTAGE TYPE)

MEMORY CELL	SELECTED/ UNSELECTED	SOURCE	DRAIN	CONTROL GATE
Q1,Q2	SELECTED	5V	0V	-10V
Q3,Q4	UNSELECTED	5V	0V	0V

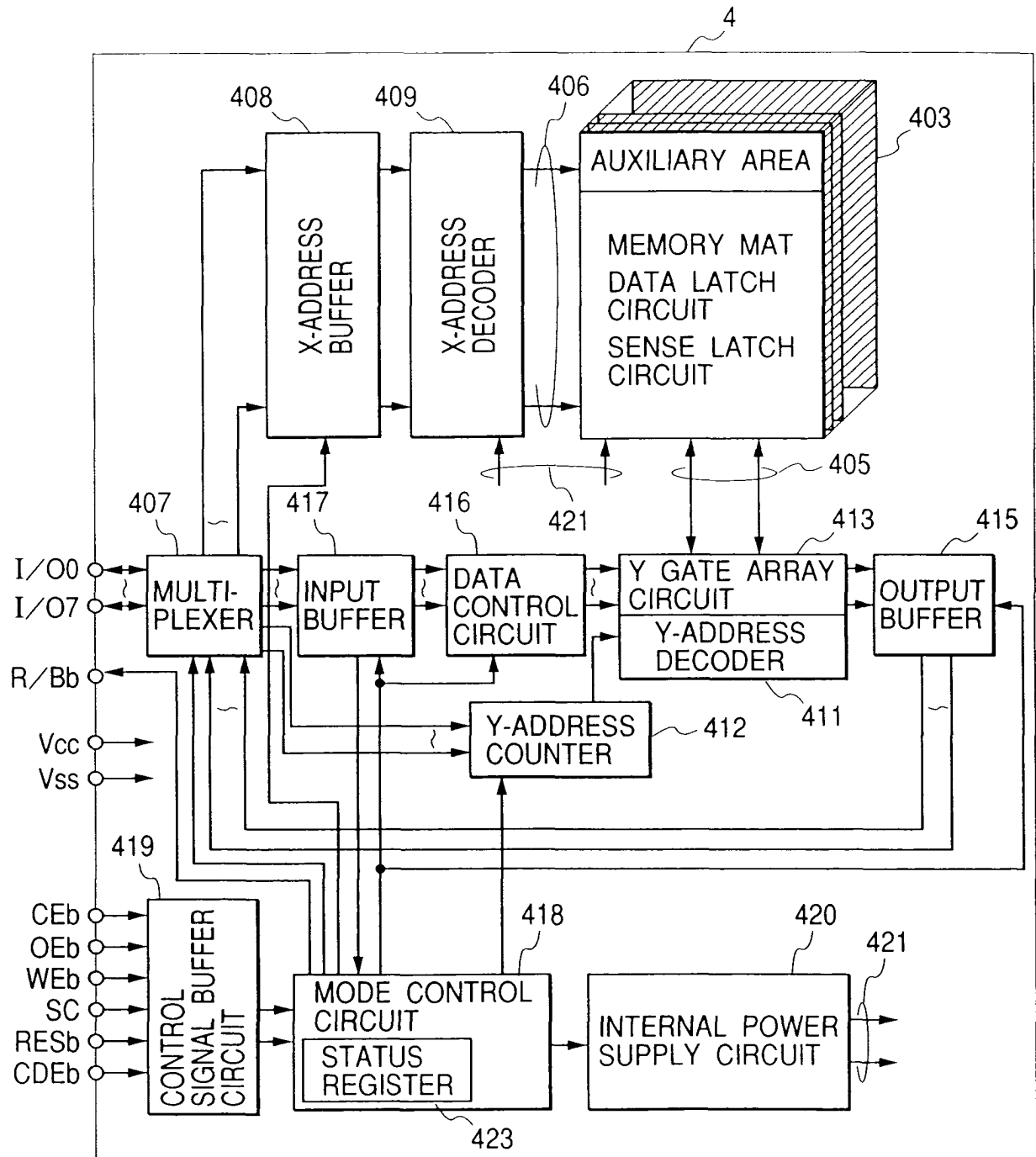
**FIG. 16**

FIG. 17

